DATA SHEET

TDA4504B
Small signal combination for multistandard colour TV

Product specification
File under Integrated Circuits, IC02

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Philips Semiconductors

PHILIPS

Small signal combination for multistandard colour TV TDA4504B

FEATURES

- Gain controlled vision IF amplifier
- Synchronous demodulator for negative and positive demodulation
- AGC detector operating on peak sync amplitude for negative demodulation and on peak white level for positive demodulation
- Tuner AGC
- AFC circuit with two control polarities and on/off-switch
- Video preamplifier
- Video switch to select either the internal video signal or an external video signal
- Horizontal oscillator and synchronization circuit with two control loops
- Vertical synchronization (divider system), ramp generator and driver with automatic amplitude adjustment for 50 and 60 Hz
- Transmitter identification (mute)
- Sandcastle pulse generation
- VCR/auto VCR switch
- Start-up circuit
- Vertical guard

GENERAL DESCRIPTION

Having the capability to demodulate IF signals with either positive or negative-going video information, the TDA4504B (Fig.1) is contained within a 32 pin encapsulation. It includes a three-stage vision IF amplifier, mute circuit, AFC and AGC circuitry, fully synchronised horizontal and vertical timebases with drive circuits and integral three-level sandcastle pulse generator.
A functional colour tv receiver can thus be realized with the addition of a tuner, audio demodulator and amplifier, chroma decoder and respective line and field deflection circuitry.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA4504B	32	DIL	plastic	SOT201(1)

Note

1. SOT201-1; 1996 November 29

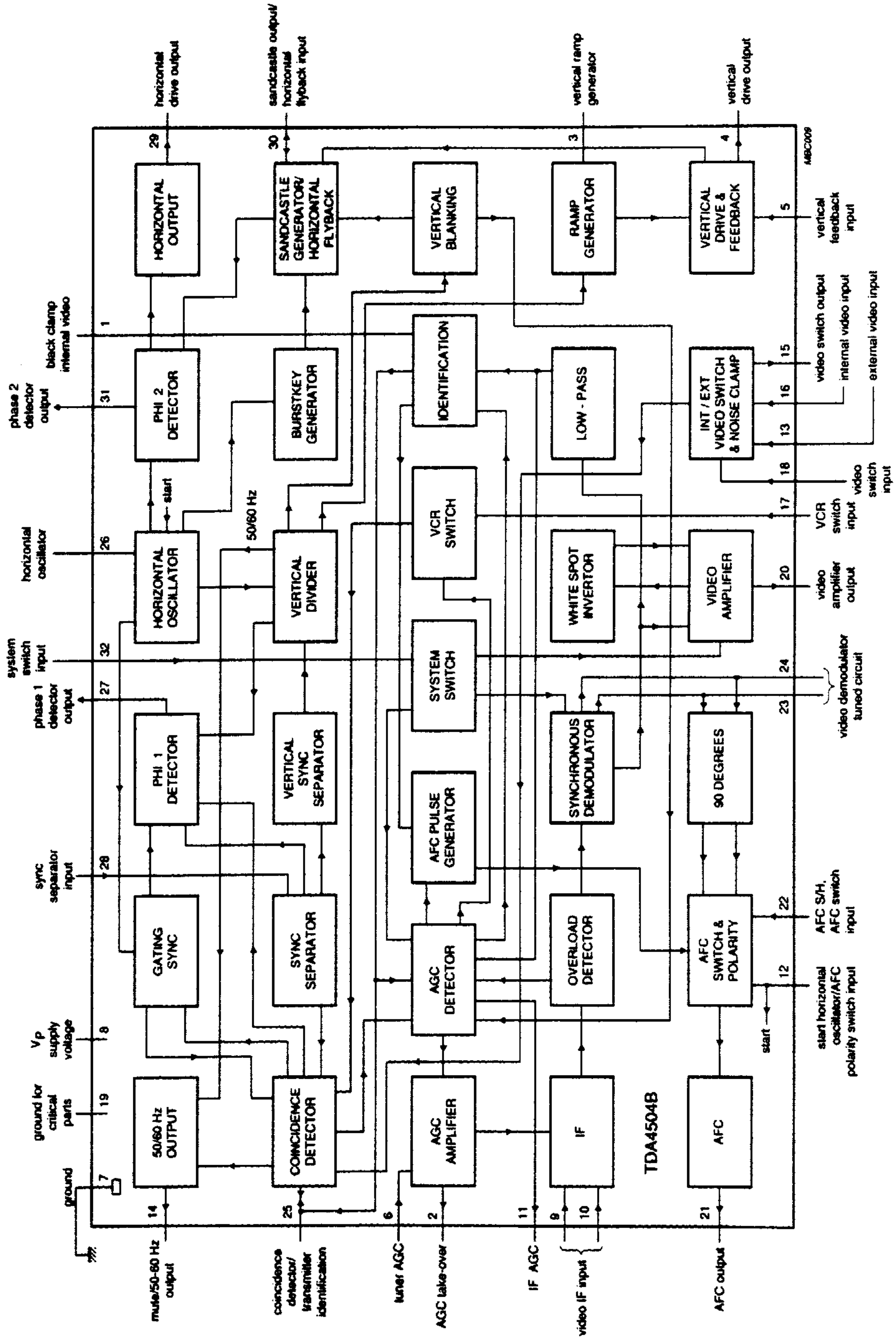


Fig.1 Block diagram.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_8	positive supply voltage pin 8		10	12	13.2	V
I_8	supply current pin 8		90	115	140	mA
I_{12}	start current pin 12		–	6.5	9	mA
Video						
$V_{9\text{-}10}$	IF sensitivity (RMS value)		25	40	65	µV
$G_{9\text{-}10}$	IF gain control range		–	74	–	dB
S/N	signal to noise ratio	V_i input signal = 10 mV	–	58	–	dB
V_{21}	AFC output voltage swing		10.5	–	11.5	V
	video output amplitude		–	2	–	V
Video switch						
$16_{(p\text{-}p)}$	internal video input		–	2	–	V
$V_{13(p\text{-}p)}$	external video input		–	1	–	V
$V_{15(p\text{-}p)}$	video output		–	2.5	–	V
Sync						
V_{28}	sync pulse input amplitude (p-p)		200	–	–	mV
I_{30}	flyback input current		0.1	–	2	mA
V_{30}	sandcastle output during burst key		8	–	–	V
	- during hor. blanking		4	4.4	5	V
	- during vert. blanking		2.1	3.3	3.7	V
V_{14}	video transmitter identification					
	- no signal condition		–	0.3	–	V
	- 50 Hz signal		–	12	–	V
	- 60 Hz signal		–	9	–	V
V_5	vert. feedback					
	- DC voltage		2.9	3.3	3.7	V
$V_{5(p\text{-}p)}$	- AC voltage		–	1	–	V

PINNING

PIN	DESCRIPTION
1	black level internal video
2	AGC take over (output)
3	vertical ramp generator (output)
4	vertical drive (output)
5	vertical feedback (input)
6	tuner AGC (input)
7	ground
8	supply voltage
9	vision IF (input)
10	vision IF (input)
11	IF AGC (output)
12	start horizontal oscillator (output)/AFC polarity switch (input)
13	external video (input)
14	mute/50 / 60 Hz (output)
15	video switch (output)
16	internal video (input)
17	VCR switch (input)
18	video switch (input)
19	ground for some critical parts
20	video amplifier (output)
21	AFC (output)
22	AFC S/H, AFC switch (input)
23	vision demodulator tuned circuit
24	vision demodulator tuned circuit
25	coincidence detector/transmitter identification
26	horizontal oscillator
27	phase 1 detector (output)
28	sync separator (input)
29	horizontal drive (output)
30	sandcastle output/horizontal flyback (input)
31	phase 2 detector (output)
32	AGC system switch (input)

FUNCTIONAL DESCRIPTION

Vision IF amplifier, demodulator and video amplifier

Each of the three AC-coupled IF stages permit the omission of DC feedback and possess a control range in excess of 20 dB.

The IF amplifier, which is completely symmetrical, is followed by a passive synchronous demodulator providing a regenerated carrier signal. This is limited by a logarithmic limiter circuit prior to its application to the demodulator.

A noise clamp circuit is provided at the video input (pin 16) to limit interference pulses below the sync tip level and is more efficient than a noise inverter in providing improved picture stability during the presence of interference.

The video amplifier has good linearity and bandwidth figures.

AFC-circuit

Obtaining the AFC reference signal from the demodulator tuned circuit presents the advantage of utilizing a single tuned circuit and one adjustment. However, since the frequency spectrum of the signal applied to the demodulator is determined by the characteristic of the SAW filter, the resultant asymmetrical spectrum with respect to the vision carrier causes the AFC output voltage to be dependent upon the video signal. The TDA4504B thus contains a sample-and-hold circuit.

With negative-going vision signals the AFC is active only during the sync pulse period. When positive-going signals are applied to the device, however, the AFC is continuously active but filtered to ensure only a small by-pass current is present in the sample-and-hold circuit.

With weak input signals the drive signal will contain considerable noise which also possesses an asymmetrical frequency spectrum and could create an offset in the AFC output voltage. The inclusion of a notch in the demodulator tuned circuit minimises this effect.

The sample-and-hold circuit is followed by a high impedance output amplifier. Thus the AFC control gradient depends upon the load impedance.

The AFC polarity switch is combined with the start circuit (pin 12). It has a negative slope when pin 12 is open or connected to the main supply and a positive slope when pin 12 is grounded. The AFC is disabled when the sample connection (pin 22) is grounded.

AGC circuit

For signals employing negative modulation the AGC detector operates on peak sync level but upon peak white content with those having positive modulation. Selection is facilitated by the system switch (pin 32):

pin 32	HIGH/open:	positive modulation
pin 32	LOW:	negative modulation

The AGC detector currents are:

	positive modulation	negative modulation
charge	1 µA	55 µA
discharge	3 mA	1.5 mA

With a 6.8 µF AGC capacitor, the video tilt will be < 10% for positively modulated signals and < 2% for negative modulation.

To obtain a rapid AGC action when executing a search tuning operation with the circuit set for peak white AGC, the charge current is held at 55 µA until the detection of a transmitted signal.

The transmitter identification

A mute signal is generated to disable the audio preamplifier of an audio demodulator during the absence of a transmission signal. When the video switch is in the internal mode, the identification of a transmitted signal is derived from the coincidence detector.
In the external mode the IF part of the circuit has its own identification system. The system relies upon the detection of sync. pulses on the incoming IF signal. The separated horizontal sync pulse charges the capacitor on pin 25 which drives the mute output (pin 14).

The connection of a 1 MΩ resistor between pin 25 and V_{CC} results in the mute information being overruled by the 50/60 Hz information derived from the internal vertical divider section
(see 50/60 Hz truth table).

MUTE Truth Table:

Input signal Pins 9 and 10	50 Hz	60 Hz	none	50/60 Hz	50/60 Hz	50/60 Hz	none
pin 25	9.5 V	9.5 V	0.3 V	9.5 V	9.5 V	9.5 V	0.3 V
pin 28	50 Hz	60 Hz	none	50 Hz	60 Hz	none	50/60 Hz
pin 18	LOW	LOW	LOW/ HIGH	HIGH	HIGH	HIGH	HIGH
pin 14	12 V	9 V	0.3 V	12 V	9 V	12 V	0.3 V

50/60 Hz Information

In the external video mode and with a resistor of 1 MΩ from pin 25 to V_{CC} the mute is overruled by the 50/60 Hz information from the divider system.

50/60 Hz Truth Table:

Input Signal	50 Hz	60 Hz	None	Don't care	Don't care	Don't care
Pin 9/10						
Pin 25	9.5	9.5	0.3	9.5	9.5	9.5
Pin 28	**50 Hz**	**60 Hz**	**None**	**50 Hz**	**60 Hz**	**None**
Pin 18	LOW	LOW	LOW	HIGH	HIGH	HIGH
Pin 14	12	9	0.3	12	9	12

VCR switch

Flywheel horizontal synchronization is desirable when receiving weak signals marred by noise but is usually unnecessary when receiving stronger off-air signals unless certain types of interference or multipath reception are apparent. Due to the inherent instability of VCR signals, however, the horizontal time constant should be shorter to prevent loss of horizontal synchronization in the early part of the scan. Provision is therefore incorporated to automatically switch the short time constant such that a strong signal instigates the 'VCR' mode and a weak signal triggers the 'TV' mode.
The connection of a switch to pin 17 provides for this to be accomplished manually and may take the form of an auxiliary switching function associated with a designated program selector button.

The TDA4504B has a separate pin (pin 17) for the VCR switch:

pin 17	HIGH:	VCR mode	fast time constant; ungated
pin 17	n.c.:	auto VCR mode	
pin 17	LOW:	TV mode	slow time constant; gated

Video-switch

Video output from the demodulator is filtered to remove the audio carrier and DC-coupled to pin 16. If AC-coupling is employed the internal noise clamp will operate on sync. tips.

The TDA4504B provides the opportunity for a direct video connection (e.g. via a peritel connector) to be made to the device at pin 13. Selection between internal and external video is made by applying a switching potential to pin 18.

Video switch:

pin 18	LOW:	internal video
pin 18	HIGH:	external video

Gain reduction

To prevent crosstalk between the IF stages and the horizontal oscillator when the device is operated in its external video mode with no RF input, the TDA4504B incorporates an option to reduce IF gain by 20 dB. This is accomplished by connecting a 39 kΩ resistor between pin 17 and ground. Omission of this component results in the IF amplifier remaining at full gain.

In the internal video mode the resistor must be disconnected to achieve the auto-VCR mode.

Horizontal synchronization

The horizontal synchronization circuit of the TDA4504B has been designed as follows:

- The retrace of the horizontal oscillator occurs during the horizontal retrace and not during the scan period. This has the advantage that no interference will be visible on the screen when receiving weak input signals. Video crosstalk will not disturb the phase of the horizontal locking.
- Reduced frequency shift of the horizontal oscillator due to noise since the horizontal phase detector reference signal is more symmetrical and independent of the supply voltage and temperature.
- The phase detector current ratio for strong and weak signals is increased to obtain a better performance during both VCR playback and weak signal reception. The switching level is also independent of temperature and supply voltage.

Vertical synchronization

Generation of the vertical sawtooth (pin 3) is accomplished by a divider that permits the production of a vertical frequency of either 50 Hz or 60 Hz with freedom from adjustment, amplitude correction and maximum interference/disturbance protection.

A discriminator window checks the vertical trigger pulse. When the trigger pulse occurs before count 576, the divider system operates in the 60 Hz mode otherwise the 50 Hz mode is selected. (2 clock pulses equal one horizontal line).

The divider section operates with different reset windows. These windows are activated via an up/down counter. This increases its count by 1 for each occasion the separated vertical sync pulse is within the selected window. On each occasion the vertical sync. pulse is not within the selected window, the count is reduced by 1.

LARGE (SEARCH) WINDOW; DIVIDER RATIO BETWEEN 488 - 722

This mode is valid for the following conditions:

1. divider locking to another transmitter
2. divider ratio found, not within the narrow window limits
3. up/down counter value of the divider system operating in narrow window mode, count falls below 10.

NARROW WINDOW; DIVIDER RATIO BETWEEN 522 - 528 (60 HZ) OR 622 - 628 (50 HZ)

The divider switches to this mode when the up/down counter has reached its maximum value of 15 approved vertical sync pulses. When the divider operates in this mode and a vertical sync pulse is missing within the window, the divider is reset at the end of the window and the count lowered by 1. At a counter value below 10, the divider switches to the large window mode.

An anti-top flutter pulse is also generated by the divider system. This inhibits the horizontal phase-1 detector during the vertical sync pulse. The width of this pulse depends upon the divider mode. For the large window mode the start is generated at the divider reset. In the narrow window mode the anti-top flutter pulse starts at the beginning of the first equalizing pulse. The anti-top flutter pulse ends at count 10 for 50 Hz and count 12 for 60 Hz.

When out-of-sync is detected by the coincidence detector, the divider is switched to count 625. This results in a stable vertical amplitude when no input signal is available.

LIMITING VALUES

In accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
T_{stg}	storage temperature range	– 55	+ 150	°C
T_{amb}	operating ambient temperature range	– 25	+ 65	°C
V_P	positive supply voltage (pin 8)	–	13.2	V
P_{tot}	total power dissipation	–	2.3	W

ESD

All pins meet:

2000 V, 100 pF, 1500 Ω

200 V, 200 pF, 0 Ω

THERMAL RESISTANCE

SYMBOL	PARAMETER	THERMAL RESISTANCE
$R_{th\ j\text{-}a}$	from junction to ambient in free air	30 K/W

CHARACTERISTICS

T_{amb} = 25 °C; supply 12 V; carrier 38.9 MHz negative modulation, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_P	supply voltage range (pin 8)		10	12	13.2	V
I_P	supply current (pin 8)	no input	90	115	140	mA
I_{12}	start current (pin 12)	note 1	–	6.5	9	mA
V_{12}	start protection level (pin 12)	I_{12} = 12 mA	–	–	16.5	V
IF Amplifier						
$V_{9-10(RMS)}$	input sensitivity (RMS–value)	note 2	25	40	65	μV
$R_{9–10}$	differential input resistance	note 3	–	1300	–	Ω
$C_{9–10}$	differential input capacitance	note 3	–	5	–	pF
$G_{9–10}$	gain control range		–	74	–	dB
ΔV_{20}	output signal expansion for 46 dB input signal variation	note 4	–	1	–	dB
V_{9-10}	maximum input signal		100	170	–	mV
V_{9-10}	input sensitivity at gain reduction	note 2	250	400	650	μV_{RMS}
Video Amplifier (note 5)						
	Zero signal output level	note 6				
V_{20}	negative modulation		4.7	4.9	5.1	V
V_{20}	positive modulation		2.5	2.7	2.9	V
V_{20}	sync tip (negative modulation)	note 7	2.5	2.7	2.9	V
V_{20}	white level (positive modulation)	note 7	4.5	4.7	4.9	V
V_{20}	white spot threshold level		–	5.5	–	V
V_{20}	white spot insertion level		–	4	–	V
Z_{20}	video output impedance		–	25	–	Ω
$I_{20(int)}$	internal bias current of NPN emitter follower output transistor		1.4	1.8	–	mA
I_{source}	maximum source current		10	–	–	mA
B	bandwidth of demodulated output signal		5	6	–	MHz
G_d	differential gain	note 8	–	2	5	%
φd	differential phase	note 8	–	2	5	°
NL	video non linearity	note 9	–	2	5	%
	intermodulation	note 10				
	1.1 MHz; blue		50	60	–	dB
	1.1 MHz; yellow		50	60	–	dB
	3.3 MHz; blue		55	65	–	dB
	3.3 MHz; yellow		55	65	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
S/N	signal-to-noise ratio	note 11 see Fig.5				
	V_i = 10 mV input signal		52	57	–	dB
	end of gain control range		57	62	–	dB
V_{20}	residual carrier signal		–	2	10	mV
V_{20}	residual 2nd harmonic of carrier signal		–	2	10	mV
AGC						
I_{C11}	allowed leakage of the AGC capacitor		–	–	700	nA
System switch (note 13)						
	AGC on sync tip level for negative modulation signals					
V_{32}	control voltage		0	–	0.8	V
I_{32}	input current		–100	–	–500	µA
	AGC on white level for positive modulation signals					
V_{32}	control voltage		2	–	12	V
I_{32}	input current		0	–	1	mA
IF sync separator						
I_I	input current		0.4	0.6	0.8	mA
I_O	output current		22	27	32	µA
V_1	clamp level		–	3.3	–	V
Tuner AGC						
$V_{9\text{-}10\ (RMS)}$	minimum starting point for tuner take-over (RMS value)		–	–	0.2	mV
$V_{9\text{-}10(RMS)}$	maximum starting point for tuner take-over (RMS value)		100	150	–	mV
I_6	maximum tuner AGC output swing	V_6 = 3 V	4	–	–	mA
V_6	output saturation voltage	I_6 = 2 mA	–	–	300	mV
I_6	leakage current		–	–	1	µA
Δ	input signal variation complete tuner control	ΔI_6 = 2 mA	0.2	2	4	dB
V_2	minimum voltage tuner take-over		–	–	1	V
Video Switching Circuit (note 14)						
EXTERNAL POSITIVE VIDEO INPUT						
$V_{13(p\text{-}p)}$	input signal (peak-to-peak value)	V_O = 2.5 $V_{(p\text{-}p)}$	–	1	–	V
I_{13}	input current		–	1.5	5	µA
V_{13}	sync tip clamping at 1 mA level		1.65	1.85	2.05	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
INTERNAL VIDEO INPUT						
16(p-p)	Internal video input signal (peak-to-peak value)	V_O = 2.5 V (p-p)	–	2	–	V
I_{16}	input current		–	1.5	5	μA
V_{16}	noise clamping at 1 mA level		2.2	2.4	2.6	V
VIDEO OUTPUT (POSITIVE VIDEO)						
$V_{15(p-p)}$	positive video output signal (peak-to-peak value)		2.3	2.5	2.7	V
V_{15}	sync tip signal		–	3	–	V
I_{bias}	internal bias current		1	1.5	–	mA
I_O	maximum output current		5	–	–	mA
α	crosstalk external to internal	notes 12 and 15	–	55	–	dB
α	crosstalk internal to external	notes 12 and 15	–	55	–	dB
Video switch						
V_{18}	input voltage for internal video		–	–	0.8	V
V_{18}	input voltage for external video		2	–	V_P	V
I_{18}	maximum current	pin 18 = 0 V	–	0.05	0.2	mA
		pin 18 = 12 V	–	0.25	1	mA
AFC-circuit (note 16)						
I_{22}	AFC sample and hold switch-off current		0.1	–	–	mA
I_O	output current	V_{22} = 0 V	0.2	0.4	0.8	mA
I_{IL}	leakage current		–	–	1	μA
V_{21}	AFC output voltage swing		10.5	–	11.5	V
I_{21}	available output current		±0.2	–	–	mA
	control slope		–	100	–	mV/kHz
V_{21}	output voltage	AFC off	5.5	6	6.5	V
R_O	AFC output resistance					
		measured at an input signal amplitude of 150 μV(RMS)	–	40	–	kΩ
$V_{21(p-p)}$	output voltage swing	note 12	–	11	–	V
	control slope	note 12	–	80	–	mV/kHz
V_{21}	output voltage shift with respect to V_I = 10 $mV_{(RMS)}$	note 12	–	–2	–	V
AFC polarity switch						
I_{12}	sink current for negative slope		–	–	1	μA
I_{12}	sink current for positive slope		0.1	–	–	mA
I_{12}	maximum current	V_{12} = 0 V	–	–	1	mA
V_{12}	switching level		5	–	7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sync separator (see Fig.6)						
V_{28}	required sync pulse amplitude	note 17	200	750	–	mV
I_{28}	input current	V_{28} = 5 V V_{28} = 0 V	– –	8 –10	– –	μA mA
First control loop						
Δf_{RX}	PLL holding range		–	±1500	±2000	Hz
Δf_{XL}	PLL catching range		±600	±1500	–	Hz
	control sensitivity to oscillator	note 18	see Fig.7			
Second control loop (positive edge)						
$\Delta td/\Delta to$	control sensitivity	note 19	–	100	–	
td	control range		–	25	–	μs
Phase adjustment (via second control loop)						
	control sensitivity		–	25	–	μA/μs
α	maximum allowed phase shift		–	±2	–	μs
Horizontal oscillator (note 19)						
f_{ft}	free running frequency	R = 34.3 kΩ C = 2.7 nF	–	15625	–	Hz
Δf_{osc}	spread with fixed external components		–	–	4	%
Δf_{osc}	frequency variations with supply voltage from 10 to 13.2 V		–	–	2	%
ΔfT	frequency variation with temperature	note 12	–	–1.6	–	Hz/K
Δf_{fr}	maximum frequency deviation at start of Horizontal output		–	–	10	%
Δf_{osc}	frequency variation when only noise is received	note 12	–	–	500	Hz
Horizontal output (open collector)						
V_{29}	output limiting voltage		–	–	16.5	V
V_{OL}	output voltage LOW	I_{sink} = 10 mA	–	0.3	0.5	V
I_{sink}	maximum sink current		10	–	–	mA
S	output signal duty factor		–	46	–	%
t_r	rise time output pulse		–	260	–	ns
t_f	fall times output pulse		–	100	–	ns
Flyback input and sandcastle output (note 22, Fig.6)						
I_{30}	required input current during flyback pulse		0.1	–	2	mA
V_{30}	output voltage during burstkey horizontal blanking during vertical blanking		 8 4 2.1	 – 4.4 2.5	 – 5 2.9	 V V V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_W	pulse width					
	burst key at:					
	60 Hz	60 Hz	2.9	3.3	3.7	μs
	50 Hz	50 Hz	3.2	3.6	4	μs
	horizontal blanking		flyback pulse			
	vertical blanking					
T_1	divider in search window	50 Hz	–	21	–	lines
		60 Hz	–	17	–	lines
T_2	divider in narrow window	50 Hz	–	25	–	lines
		60 Hz	–	21	–	lines
	delay between the start of the sync pulse at the video output and the burst key pulse					
t_{Bkt}	trailing edge	60 Hz	–	–	9.4	μs
t_{Bkr}	rising edge		4.7	5.4	6.1	μs
VCR switch (non-VCR mode; V_{17} < 5 V)						
R_{17}	resistance to ground		–	–	5	kΩ
I_{17}	output current	pin 17 = 0 V	–	–	0.5	mA
VCR switch (auto-VCR mode)						
I_{17}	source current		–	–	30	μA
I_{17}	sink current		–	–	30	μA
VCR switch (VCR mode; V_{17} > 7 V)						
R_{17}	resistance to V_{CC}		–	–	5	kΩ
I_{17}	input current	$V_{17} = V_{CC}$	–	–	1	mA
$V_{9-10(rms)}$	IF input signal for switching from fast to slow in auto VCR mode (RMS value)		–	2.2	–	mV
Vertical ramp generator (note 21)						
I_3	input current during scan		–	–	2	μA
I_3	discharge current during retrace		–	0.8	–	mA
$V_{3(p-p)}$	sawtooth amplitude (peak-to-peak value)		–	1.9	–	V
t	interlace timing of the internal pulses	note 12	30	32	34	μs
Vertical output						
I_4	available output current	V_4 = 4 V	–	–	3	mA
V_4	maximum available output voltage	I_4 = 0.1 mA	4.4	5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Vertical feedback input						
v_5	DC input voltage		2.9	3.3	3.7	V
$V_{5(p-p)}$	AC input voltage (peak-to-peak value)		–	1	–	V
I_5	input current		–	–	12	μA
Δ_{tp}	internal pre-correction to sawtooth		–	3	–	%
	deviation amplitude	50/60 Hz	–	–	2	%
	temperature dependency of the amplitude	note 12 ΔT = 45 °C	–	–	2	%
Vertical guard ($V_{pin\ 30}$ = 2.5 V)						
ΔV_5	active switch level at a deviation with respect to the DC feedback level	note 22				
	guard level LOW		–	1.5	–	V
	guard level HIGH		–	2	–	V
Coincidence detector/transmitter identification (note 23)						
V_{25}	voltage for in-sync condition		–	9.8	–	V
V_{25}	voltage for no-sync condition	no signal	–	0.3	–	V
V_{25}	switching level to switch the phase detector from fast to slow		6.2	6.7	7.2	V
V_{25}	hysteresis slow to fast		–	0.6	–	V
V_{25}	switching level to activate the mute function (transmitter identification)		2.5	2.8	3.1	V
V_{25}	hysteresis mute function		–	2.5	–	V
Video transmitter identification output						
V_{14}	output voltage active	no sync; I = 1 mA	–	0.3	0.5	V
I_{14}	sink current active		–	–	5	mA
I_{14}	output current inactive (transmitter present)		–	–	1	μA
50/60 Hz identification (note 24)						
V_{14}	output voltage at 50 Hz		–	V_s	–	V
V_{14}	output voltage at 60 Hz		–	9	–	V

Notes to the characteristics

1. Supplying a current of 9 mA to pin 12 starts the horizontal oscillator. This current can be obtained via a bleed circuit from the mains rectifier whilst the main supply for the device (V_P) is obtained from the horizontal output stage. The load current of the driver must be added to the value given above.
2. On set AGC.
3. The input impedance has been chosen such that a SAW filter can be employed.
4. Measured with 0 dB = 450 μV.
5. Measured at 10 mV (RMS) 100% input signal.
6. Projected zero point; i.e. with switched demodulator.
7. The output signal amplitude is determined by the AGC detector. For negative modulation the sync tip level is used as reference. With positive modulation the white level is stabilized
8. Measured according to the test line given in Fig.3.
   a) The differential gain is expressed as a percentage of the difference in peak amplitudes between the largest and smallest value relative to the subcarrier amplitude at blanking level.
   b) The differential phase is defined as the difference in degrees between the largest and smallest phase angle.
   c) The differential gain and phase are measured with a DSB signal.
9. This figure is valid for the complete video signal amplitude (peak white to black). The non-linearity is expressed as a percentage of the maximum deviation of a luminance step from the mean step, with respect to the mean step.
10. The test set-up and input conditions are given in Fig.5. The figures are measured at an input signal of 10 mV (RMS).
11. Measure with a source impedance of 75 Ω. The signal-to-noise ratio =

$$20\ \log \frac{V_o \text{ black-to-white}}{V_{n\,(RMS)} \text{ at B = 5 MHz}}$$

12. These figures are based on sample tests.
13. By means of the system switch, two conditions can be obtained. Negative modulation with sync tip level AGC. This is obtained with pin 32 connected to ground. Positive modulation with peak white AGC. This is obtained with pin 32 connected to the positive supply.
14. When the video switch is in the external mode the first control loop in the synchronization circuit is not switched to a long time constant when weak signals are received.
15. Defined as $(20\ \log)\ \frac{V_o \text{ unwanted video black-to-white}}{V_o \text{ wanted video-black-to-white}}$; measured at 4.4 MHz.
16. The indicated figures are measured at an input signal of 10 mV RMS. The unloaded Q-factor of the reference tuned circuit is 70.
    With very weak input signals the drive signal for the AFC circuit will have a high noise content. This noise input has a asymmetrical frequency spectrum which will cause an offset of the AFC output voltage. To avoid problems due to this effect a notch filter can be built into the demodulator tuned circuit. The characteristics given for weak signals are measured without a notch circuit, with a SAW filter connected in front of the IC input signal such that the input signal of the IC is 150 μV (RMS value).
17. The minimum value is obtained by connecting a 1.8 kΩ resistor between pins 15 and 28. The slicing level can be varied by changing the value of this resistor (higher resistor value results in larger value of the minimum sync pulse amplitude). The slicing level is independent of the video information.
18. Frequency control is obtained by supplying a correction current to the oscillator RC network via a resistor connected between the phase 1 detector output and the oscillator network. The oscillator can be adjusted to the correct frequency by short circuiting the sync separator bias network (pin 28) to $+V_P$. To avoid the need of a VCR switch the time constant of the phase detector at strong input signals is sufficiently short to get a stable picture during VCR playback. During the vertical retrace period the time constant is even shorter so that the head-errors of the VCR are

compensated at the beginning of scan. During conditions of weak signal (information derived from the AGC circuit) the time constant is increased to obtain a better noise immunity.

19. This figure is valid for an external load impedance of 82 Ω from pin 31 to the shift adjustment potentiometer.
20. The flyback input and sandcastle output have been combined on one pin. The flyback pulse is clamped to a level of 4.5 V. The minimum current to drive the second control loop is 0.1 mA.
21. The vertical scan is synchronized by means of a divider system. Therefore no adjustment is required for the ramp generator. The divider detects whether the incoming signal has a vertical frequency of 50 or 60 Hz and corrects the vertical amplitude.
22. To avoid CRT screen burn due to a collapse of the vertical deflection a continuous blanking level is inserted in the sandcastle pulse when the feedback voltage of the vertical deflection is not within the specified limits.
23. The functions in-sync/out-of-sync and transmitter identification have been combined on this pin.
    The capacitor is charged during the sync pulse and discharged during the time difference between gating (6.5 / µs) and the sync pulse in the internal video mode. When the circuit is in the external mode the capacitor is charged by the horizontal sync pulse and discharged continuously with a small current.
24. When the mute is active no 50/60 Hz information is available.

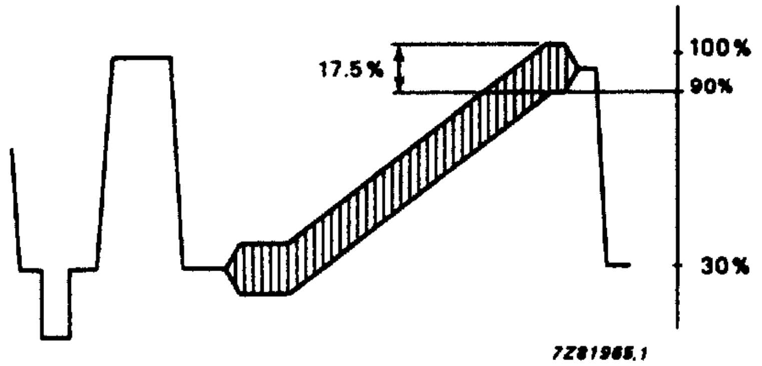


Fig.2 Video output signal.

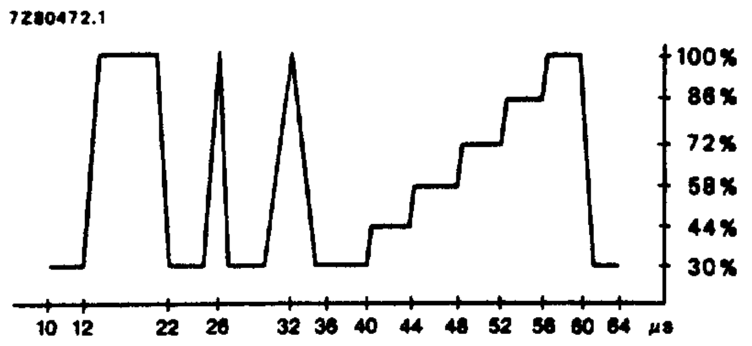
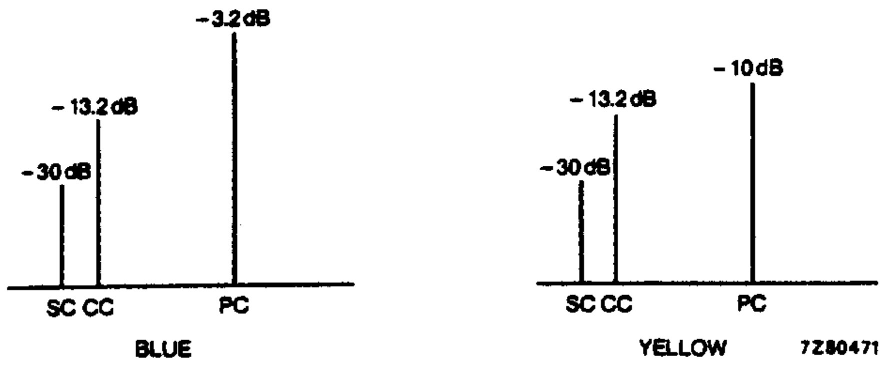
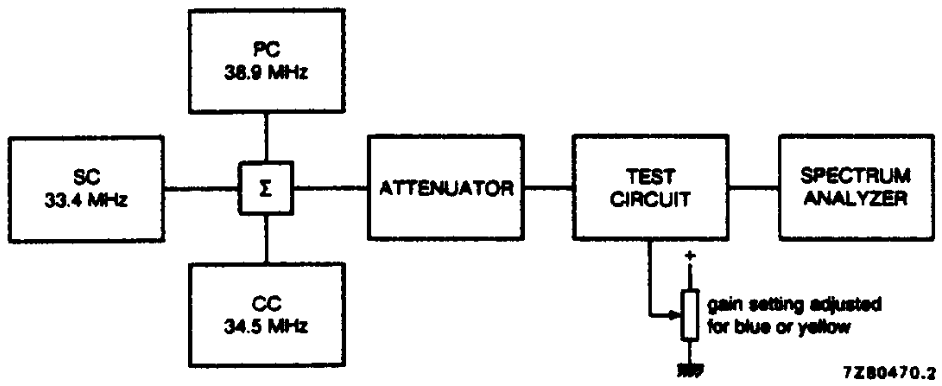


Fig.3 EBU test signal waveform (line 17).





Input signal conditions
SC = Sound carrier
CC = Chrominance carrier
PC = Picture carrier
All with respect to top sync level

Value at 1.1 MHz : $20\ \log\frac{V_o \text{ at } 4.4\text{MHz}}{V_o \text{ at } 1.1\text{MHz}} + 3.6\text{dB}$

Value at 3.3MHz : $20\ \log\frac{V_o \text{ at } 4.4\text{MHz}}{V_o \text{ at } 3.3\text{MHz}}$

Fig.4 Test set-up intermodulation.

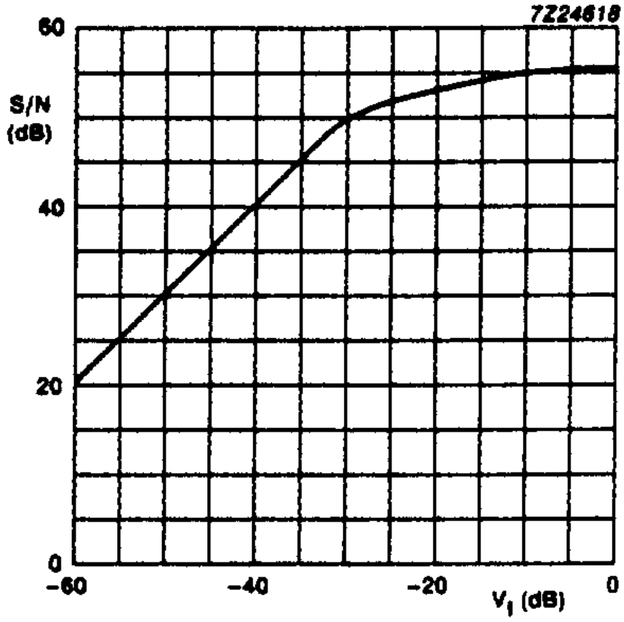
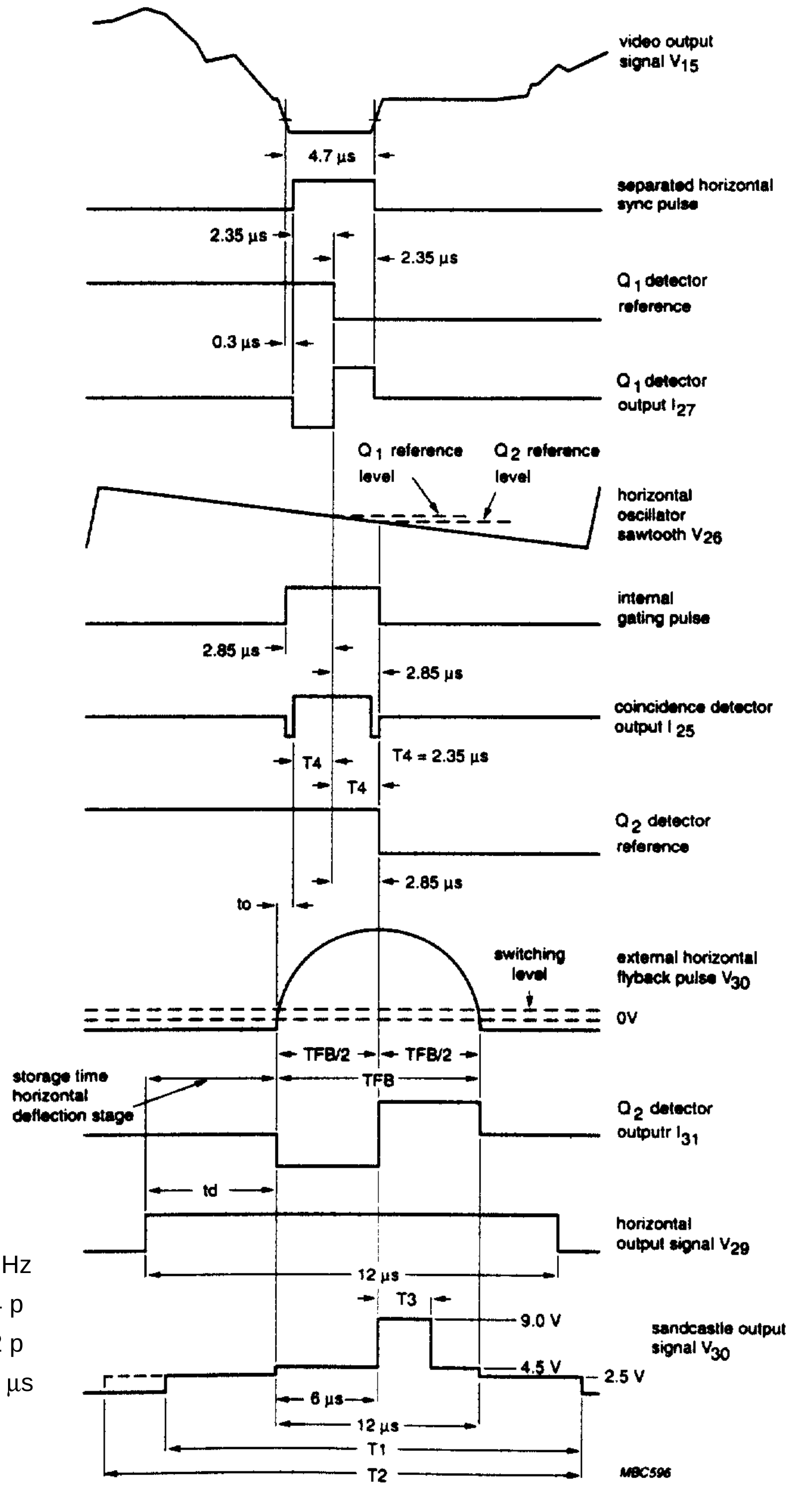


Fig.5 Signal-to noise ratio as a function of the input voltage (0 dB = 100 mV).



		50 Hz	60 Hz
T_1 -	search window -	42 p	34 p
T_2 -	narrow window -	50 p	42 p
T_3 -	burst key pulse -	3.6 μs	3.3 μs

$$\left(p = \frac{1}{2f_H}\right)$$

Fig.6 Timing diagram.

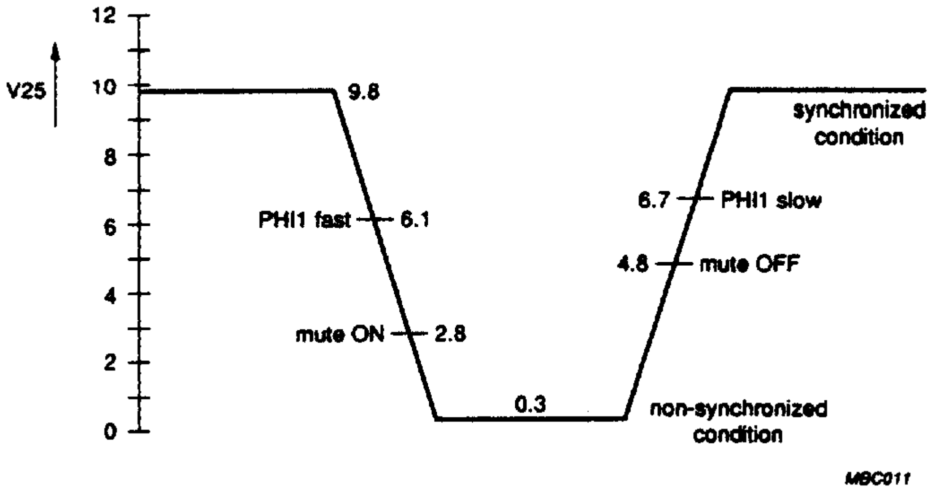


Fig.7 Switching levels coincidence detector.

COINCIDENCE DETECTOR SWITCHING LEVELS

CONDITION PIN 18 VIDEO SWITCH	CONDITION PIN 17 VCR SWITCH	CONDITION V_{25}	CONTROL SENSITIVITY HOR.OSCILLATOR kHz / μS	
			T2 – T1	T3 = SCAN
Low internal video	floating automatic VCR	V_{25} >6.7 V and		
		strong signal	11.3	7.6
		weak signal	1.3	1.3
		V_{25} < 6.1 V and		
		strong signal	11.3	7.6
		weak signal	11.3	7.6
	HIGH forced VCR	don't care	11.3	7.6
	LOW T.V. mode	V_{25} > 6.7 V V_{25} < 6.1 V	1.3 11.3	1.3 7.6
HIGH or floating external video	don't care	don't care	11.3	7.6

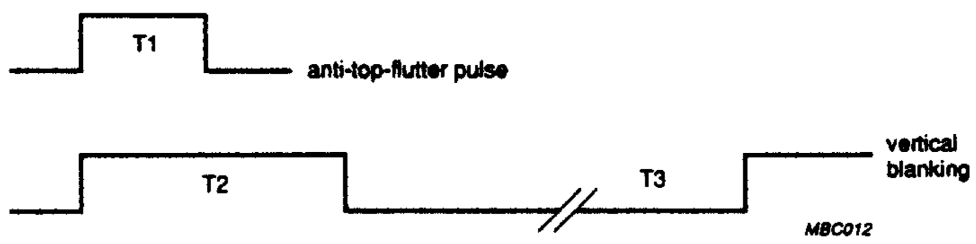


Fig.8 Horizontal oscillator control sensitivity.

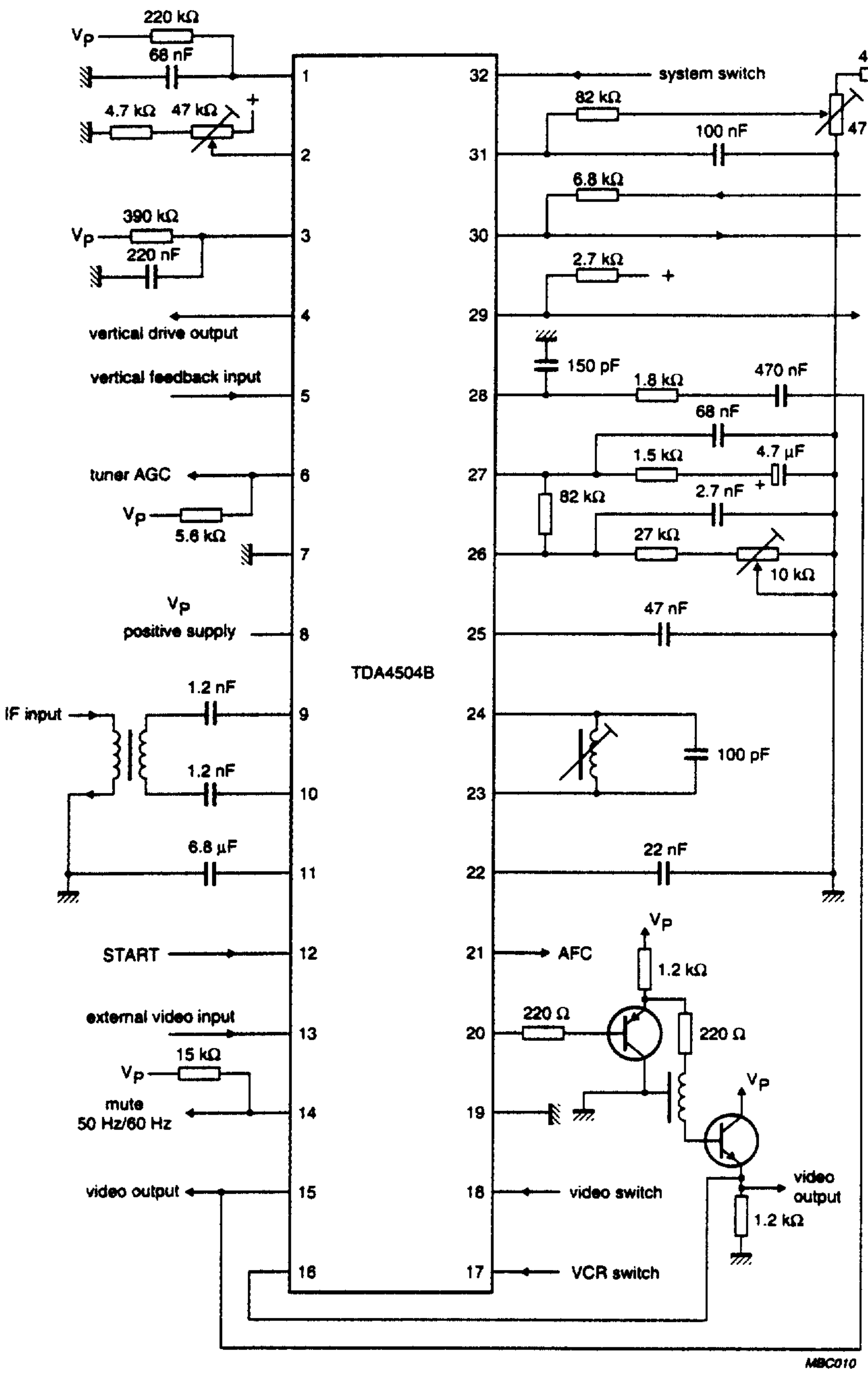
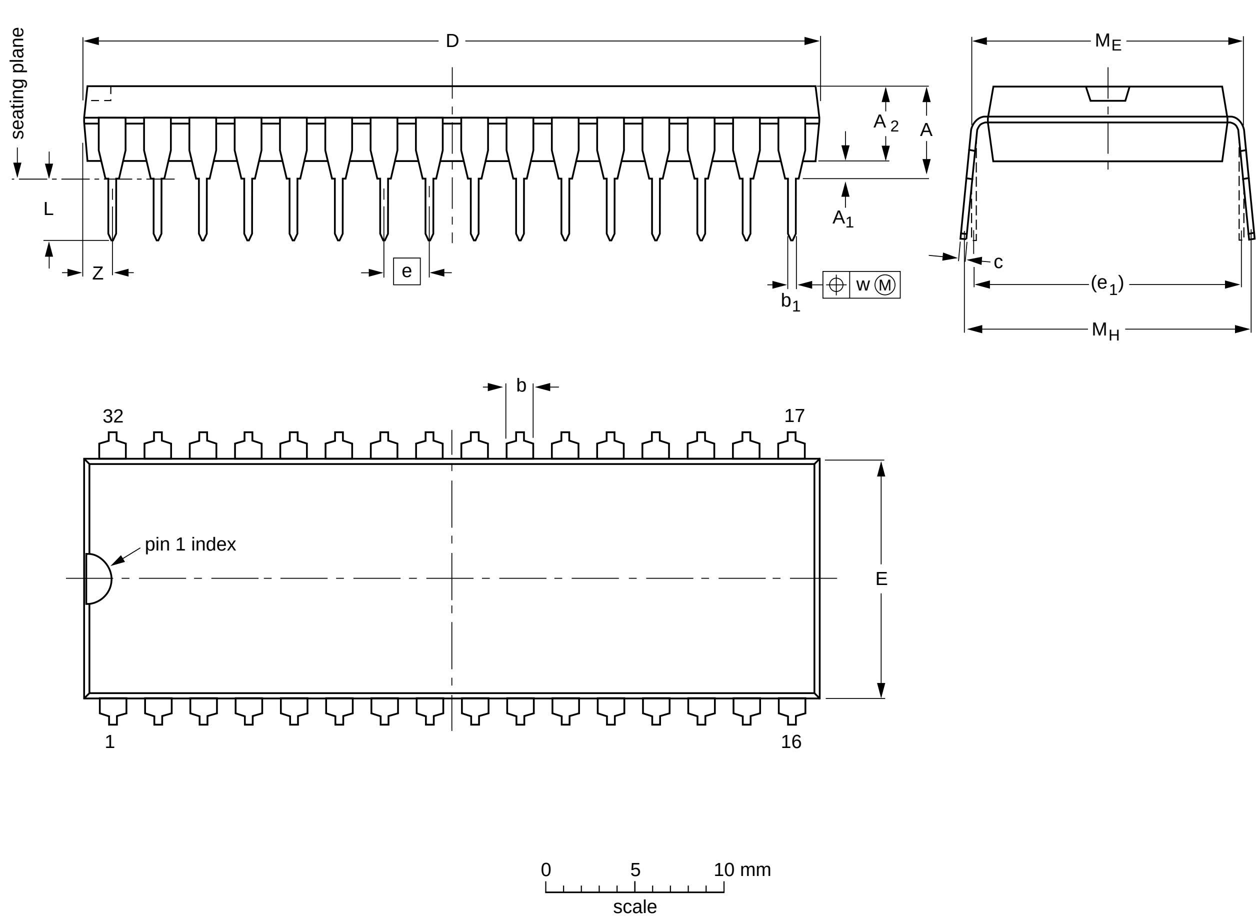


Fig.9 Application diagram.

PACKAGE OUTLINE

DIP32: plastic dual in-line package; 32 leads (600 mil) **SOT201-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	5.0	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	41.6 40.6	14.2 13.8	2.54	15.24	3.6 3.2	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.64 1.60	0.56 0.54	0.10	0.60	0.14 0.13	0.62 0.60	0.68 0.63	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT201-1						~~90-01-22~~ 95-01-25

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.